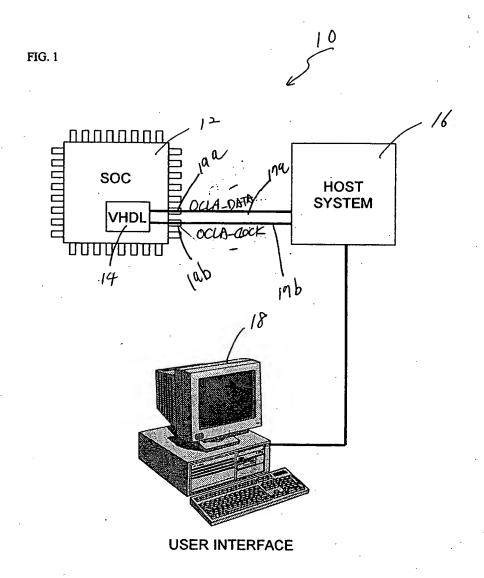


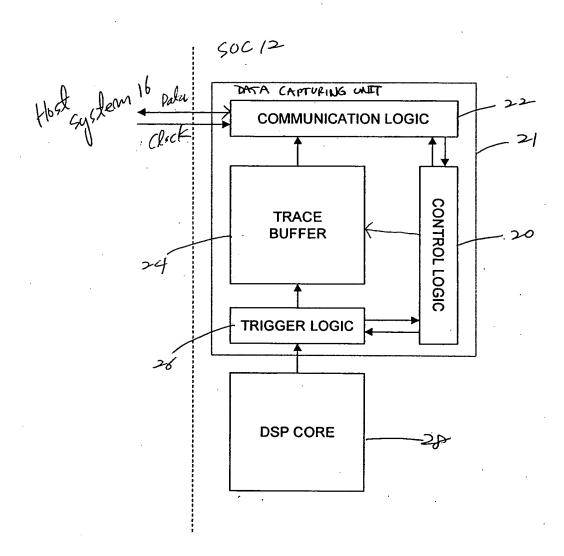


Figures

APP_ID=09683091

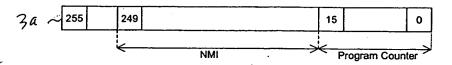
(RAH) BUR920000199US1 William S. Corti et al. 1 of 6

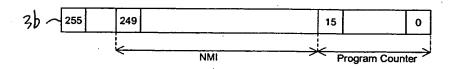


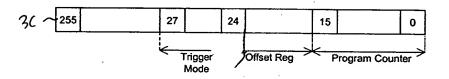


BUR920000199US1 William S. Corti et al. 3 of 6

FIG. 3



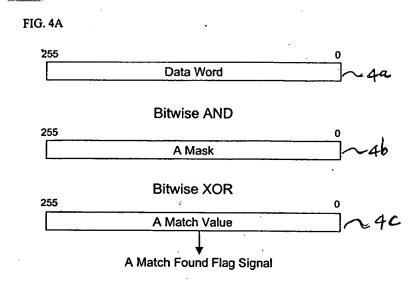


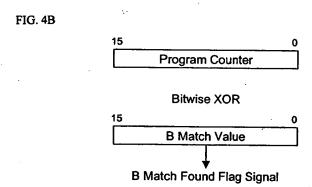


	Trigger Modes	4 Bits
3d	Trigger on A	"0000"h
	Trigger on B	"0001"h
	Trigger on A or B	"0010"h
	Trigger on A Then B	"0011"h
	Trigger on B Then A	"0100"h
	Trigger on A or B	"0101"h
	·	

3e –	Extra Data Bus Mux Selection	4 Bits
	Data Write Address & Data Write External Data Bus Mux	"0000"h "0001"h

BUR920000199US1 William S. Corti et al. 4 of 6





BUR920000199US1 William S. Corti et al. 5 of 6

FIG. 5A

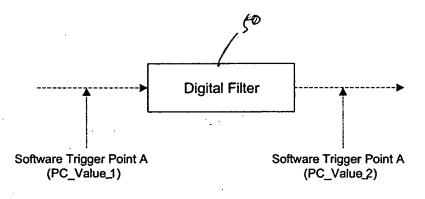


FIG. 5B

PC	Label	Label
1000	PC_Value_1	LOAD input into a DSP Register
1002	1002	LOAD starting point of addressing registers
1004	1004	LOAD repeat loop register with N
1006	1006	CLEAR multiply accumulate register
1008	1008	MULTIPLY-ACCUMULATE N times, update pointers
100A	100A	SHIFT to normalize result
100C	PC_Value_2	STORE result

BUR920000199US1 William S. Corti et al. 6 of 6

FIG. 6

